**ELEC 204 Digital Design Preliminary Lab Report**

Preliminary Lab 4

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\*Please delete the highlighted lines and write your own parts for the report.

\*\*Reminder: Your lab grade is a weighted average of your performance before, during and after the lab: **Total lab grade = Preliminary work\* (30%) + Lab interview and demo\* (40%) + Lab report (30%)**

**\*\*\*Please make sure the preliminary report does not exceed 2 A4 pages.**

For the preliminary work, please provide here:

* *Your answers to the questions in the tutorial lab*

1. *To see the multiplexing of seven segment, we can lower the clock frequency to 1Hz (period = 1s). We can use a clock divider circuit to lower the frequency. We, basically, take the master clock and create a new clock. For accomplishing this goal, we can use a counter and count the rising edges of the master clock. When counter reaches the number which we will divide our clock with minus 1, we set the new clock to be 1 and keep it 0 otherwise. When clock reaches the designated number, counter resets to 0. In our case, we want to divide our clock with 1.000.000 to lower its frequency from 100 MHz to 1Hz. Therefore we will reset the counter when it reaches 99.999.999 (x”5F5E0FF”)  
     
   Here is the code:  
   Counter = x(0000000) ;   
   N = x(5F5E0FF);   
   if rising\_edge(MCLK)*

*Counter <= counter + x(0000001);   
 new\_CLK <= ‘0’;   
 If counter == N   
 new\_CLK <= ‘1’   
 Counter <= ‘0’;*

*End if   
End if*

1. *We reset the counter every time when it reaches N. Since counter goes from 0 to N, it takes N+1 step to become 1. Therefore slower clock is N+1 times less frequent than the master clock:  
     
   FM = (N+1)\*FD*
2. *N is “5F5E0FF” in hex form as explained above. If we convert this number to binary, it becomes “101 1111 0101 1110 0000 1111 1111”. Therefore, we need 27 bits to represent N.*